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10/633,641	08/05/2003	Eung Tae Kim	0465-1045P	5457

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EXAMINER	
HUBER, JEREMIAH C	

ART UNIT	PAPER NUMBER
2621	

NOTIFICATION DATE	DELIVERY MODE
09/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/633,641	KIM, EUNG TAE	
	Examiner	Art Unit	
	Jeremiah C. Huber	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6, 8 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Lane (5598222) and Boyce et al (5635985) which is incorporated by reference in Lane (Lane col. 3 lines 47-50) in view of Lyu (20010007576).

In regard to claims 1-2 Lane disclose a video decoding system including:

a plurality of transport decoders for receiving compressed bitstreams of a plurality of channels, parsing and outputting the respective video bitstreams (Lane Fig. 1 12 and 14 and col. 3 lines 1-34);

a video decoder for receiving the HD-class video bitstreams of the plurality of channels through the transport decoders, and decoding a plurality of video frames for a display frame period in the unit of a picture (Lane Fig. 1 20 col. 3 lines 35 to 50 and col. 4 lines 31 to 39 also see Boyce Figs. 2A&B and col. 4 lines 55-63 and col. 19 lines 15-

23 note Boyce discloses that the primary decoder can decode HD streams, Lane discloses that the secondary decoder can receive HD streams);

an external memory for storing video-decoded frames for a motion compensation in the video decoder and a dual video display (Lane Fig. 1 18 and col. 3 lines 51-59);

a video display processor (VDP) for reading out the video frame data of the plurality of channels decoded by the video decoder from the external memory, converting the video frame data to match a display format, and simultaneously displaying the video frame of the plurality of channels on a screen of a display device (Lane Fig. 1 22 and col. 3 line 60 to col. 4 line 2 note display formats are PIP and non-PIP); and

a memory interface for interfacing the video decoder, the external memory and the VDP so that the video decoder decodes and displays the plurality of HD-class video frames for the display frame period (Lane Fig. 1 24 and col. 3 lines 51-59).

a video buffer for temporarily storing the video bitstreams of the plurality of channels outputted through the plurality of TS decoders in the unit of a picture, and then outputting the video bitstreams (Lane Fig. 1 18 and col. 3 lines 51-59 and Boyce Figs. 2A&B 116 and col. 5 lines 7-14 note Lane discloses a single memory for plural decoders, Boyce discloses that the memory is structured into a buffer and a frame memory);

variable-length decoder (VLD) units for separating the video bitstreams of the plurality of channels outputted through the video buffer into motion vectors, quantization values, and DCT coefficients by variable-length-decoding the video bitstreams in the

unit of a picture (Lane Fig. 1 20 col. 3 lines 35 to 50 and col. 4 lines 31 to 39 also see Boyce Figs. 2A&B and 4 note 120 and col. 4 line 64 to col. 5 line 3 and col. 17 line 6 66 to col. 18 line 38 note the PIP decoder would include two VLD circuits one for each decoder);

a plurality of inverse quantization (IQ) units for inverse-quantizing the DCT coefficients of the respective channels in accordance with the corresponding quantization values (Lane Fig. 1 20 col. 3 lines 35 to 50 and col. 4 lines 31 to 39 also see Boyce Figs. 2A&B and 4 note 122 and col. 4 line 64 to col. 5 line 3 and col. 18 lines 50 to 54 discusses details of two IQ's);

A plurality of inverse discrete cosine transform (IDCT) units for receiving the DCT coefficients inverse-quantized by the IQ unit, dividing sub-blocks in a macro block including the inverse-quantized DCT coefficients into a plurality of groups and performing a pipelined IDCT of the group (Lane Fig. 1 20 col. 3 lines 35 to 50 and col. 4 lines 31 to 39 also see Boyce Figs. 2A&B and 4 note 124 and col. 4 line 64 to col. 5 line 3 and col. 18 lines 39 to 49 discusses details of two IDCT's);

motion compensation units for performing motion compensation of present pixel values in the unit of a picture using the motion vectors outputted form the VLD unit and a previous frame stored in the external memory (Lane Fig. 1 20 col. 3 lines 35 to 50 and col. 4 lines 31 to 39 also see Boyce Figs. 2A&B and 4 note 130 and col. 4 line 64 to col. 5 line 3 and col. 17 line 6 66 to col. 18 line 38 note the PIP decoder would include two motion compensation circuits one for each decoder) ; and

adders for adding IDCT-transformed values outputted from the respective IDCT units and motion-compensated values outputted from the motion compensation unit (Lane Fig. 1 20 col. 3 lines 35 to 50 and col. 4 lines 31 to 39 also see Boyce Figs. 2A&B and 4 note 128 and col. 4 line 64 to col. 5 line 3 and col. 17 line 6 66 to col. 18 line 38 note the PIP decoder would include two adder circuits one for each decoder).

It is noted that neither Lane nor Boyce disclose using single circuits to implement variable length decoding, motion compensation, and adding functions for plural bitstreams or a picture control unit. However, Lyu discloses a decoding device (Lyu Fig. 1 and pars. 19-21) that uses single circuits to implement variable length decoding, motion compensation and adding for plural bitstreams (Lyu Fig. 1 102-2, 102-6 and 102-7 and pars. 19-20). Lyu further discloses a picture control unit for controlling decoding processes (Lyu Fig. 1 105 and par. 21). Lyu also discloses that the single circuits operate on plural channels by alternately decoding frames from respective channels, (Lyu par. 23 note time multiplexing alternately applies video bitstreams to decoding elements also note multi display controlling part 106). It is therefore considered obvious that one of ordinary skill in the art would recognize the advantage of modifying Lane and Boyce to include the shared component and control aspects of Lyu in order to make use of surplus processing capability as disclosed by Lyu (Lyu par. 19). One would further see the benefit of not sharing the IQ and IDCT components as secondary IQ and IDCT components can be less complex as is disclosed by Boyce (Boyce col. 18 lines 39 to 54).

In regard to claim 3 refer to the statements made in regard to claim 2 above. Lane discloses the use of two transport decoders (Lane Fig. 1 12 and 14) and two decoders (Lane Fig. 1 17 and 19) which will each contain an IQ and an IDCT (Boyce Figs. 2A&B note 122 and 124).

In regard to claim 4 refer to the statements made in the rejection of claim 3 above. Lane and Boyce further disclose a down-sampling unit for performing a reduction of an output of the adder in horizontal and vertical directions according to picture and display types and storing the reduced data in the external memory (Lane fig. 1 15 and col. 3 lines 35 to 59, note pre-parser will reduce data input and output to the entirety of the reduced resolution decoder, for the picture to be displayed as the inset picture); and

an up-sampling unit for up-sampling data readout from the memory in a horizontal direction during motion compensation and outputting the up-sampled data to the motion compensation unit (Boyce Figs. 2 A&B 131).

In regard to claims 5-6 refer to the statements made in the rejection of claim 4 above. Lane and Boyce further disclose ½ reduction of resolution of the respective pictures in the horizontal and vertical directions in accordance with display type of the data outputted from the adder, particularly reducing the resolution by ½ for the sub-picture and not the main picture (Lane col. 4 line 63 to col. 5 line 16 note ½ reduction for the reduced resolution inset picture).

In regard to claim 8 refer to the statements made in the rejection of claims 1 and 2 above. Lyu further discloses that the picture control unit can control the decoder to

decode one frame of video per half period of a field display period (Lyu Fig. 3 note one frame of video (i.e. vid0 0T&0B) are decoded per half cycle of disp_sync). The examiner believes this meets the definition of setting a decode_sync signal to a half period of a disp_field signal as decode_sync and disp_field are defined in the specification in par. 57.

In regard to claim 10 refer to the statements made in the rejection of claim 1 above. Boyce further discloses the use of SDRAM (Boyce col. 5 lines 7-14 note synchronous DRAM). It is noted that neither Lane, Boyce nor Lyu explicitly disclose the use of a 64 bit double data (DDR) rate SDRAM operating at a frequency of at least, 135MHz as an external memory. However, the examiner takes official notice that the use of DDR SDRAM with a wide range of bit widths and operating frequencies were common and notoriously well known in the art of computing at the time of the invention, and that it would therefore have been obvious for one of ordinary skill in the art to incorporate a DDR SDRAM according to the applicant's specifications in the invention of Lane and Boyce in view of Lyu in order to provide a low cost, high bandwidth external memory. It is noted that the applicant did not traverse the official notice taken by the examiner with regard to this claim in the previous action, it is therefore considered as admitted prior art See MPEP 2144.03 part C.

In regard to claim 11 refer to the statements made in the rejection of claim 1 above. Lyu further discloses that the single circuits operate on plural channels by alternately decoding video from the respective channels (Lyu par. 23 note time multiplexing alternately applies video bitstreams to decoding elements).

In regard to claim 12 refer to the statements made in the rejection of claim 1 above Lane and Boyce further discloses that decoding is performed on the channels without reduction of resolution of the video bistreams (Lane Fig. 1 note decoders 12 and 14 operate to decode a video bit stream from a compressed stream at full resolution).

2. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lane and Boyce in view of Lyu as applied to claim 4 above, and further in view of Yoon (6226039).

It is noted that neither Lane, Boyce nor Lyu disclose details related to a split screen type display. However Yoon discloses an aspect ratio conversion apparatus in which main and sub channel images are sub-sampled by ½ in the horizontal direction for use in a split screen display (Yoon Figs3-5 and col. 3 lines 23-37). It is therefore considered obvious that one of ordinary skill in the art at the time of the invention would recognize the advantage of including split screen display capability as disclosed by Yoon in the invention of Lane and Boyce in view of Lyu in order to display the main and sub channel images in approximately equal proportion.

3. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lane and Boyce in view of Lyu and in further view of design choice.

Lane and Boyce in view of Lyu discloses decoding a frame from each of two channels during one field period (hereafter T-B-T-B configuration) as stated in the rejection of claim 8 above.

Lane and Boyce in view of Lyu does not disclose expressly decoding the top fields of each channel during the first half of a field period, and decoding the bottom fields of each channel during the second half of each field period (hereafter T-T-B-B configuration).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to decode channels in a T-T-B-B configuration. Applicant has not disclosed that the T-T-B-B configuration provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a T-B-T-B configuration because the processing requirements are approximately the same.

Therefore, it would have been obvious to one of ordinary skill in this art to modify Lane and Boyce in view of Lyu to include a T-T-B-B configuration in order to obtain the invention as specified in claim 9.

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kempisty discloses a video decoding system with plural transport decoders and a video decoder that alternately decodes the respective channels.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremiah C. Huber whose telephone number is (571)272-5248. The examiner can normally be reached on Mon-Fri 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571)272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremiah C Huber
Examiner
Art Unit 2621

Mehrdad Dastouri

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